REMARKS

Claims 1-62 are canceled, and new claims 63-84 are added.

The subject matter of claims 63-84 is fully supported by the originally-filed application, and therefore does not comprise "new matter". For instance, claim 63 is fully supported by Fig. 1 of the application as follows:

a substrate -- shown in Fig. 1 as substrate 12;

a pair of wordlines supported by the substrate; the wordlines each comprising a gate dielectric, an electrically conductive material and an electrically insulating cap; the electrically insulative caps of the wordlines having uppermost surfaces -- the wordlines are shown in Fig. 1 as 14 and 16, with each of the wordlines comprising gate dielectric 18, electrically conductive material 20, and electrically insulating caps 22;

a source/drain region within the substrate between the wordlines, the source/drain region being electrically isolated from one of the wordlines and being part of a transistor comprising a gate contained by the other of the wordlines -- the source/drain region shown in Fig. 1 as 26;

an electrically conductive pedestal between the wordlines, over the source/drain region, and electrically connected with the source/drain region; the electrically conductive pedestal having an uppermost surface; the uppermost surface of the conductive pedestal and the uppermost surfaces of the electrically insulative caps of the wordlines together forming a planar platform extending across the wordlines and the electrically conductive pedestal -- the electrically conductive pedestal is shown in Fig. 1 as 32; and is shown

having an uppermost surface that, together with uppermost surfaces of insulating caps 22, forms a planar platform extending across the pedestal and wordlines;

a first capacitor electrode over the planar platform and having a planar surface of conductively-doped silicon -- shown in Fig. 1 as 34, and described in paragraph 0027 as comprising conductively-doped silicon in some aspects of the invention;

a planar second capacitor electrode over the first capacitor electrode planar surface and comprising one or more materials selected from the group consisting of metals and metal compounds -- shown in Fig. 1 as 40, and described in paragraph 0035 as comprising metal and/or metal compounds in some aspects of the invention;

a planar first dielectric layer between the first and second capacitor electrodes, the first dielectric layer comprising aluminum oxide -- shown in Fig. 1 as 36, and described in paragraph 0029 as comprising aluminum oxide in some aspects of the invention;

a planar second dielectric layer between the first and second capacitor electrodes, the second dielectric layer comprising a metal oxide other than aluminum oxide -- shown in Fig. 1 as 38, and described in paragraph 0030 as comprising metal oxide other than aluminum oxide in some aspects of the invention;

wherein the first dielectric layer is between the second dielectric layer and the conductively-doped silicon -- shown in the aspect of the invention of Fig. 1;

wherein the metal oxide of the second dielectric layer is in physical contact with the second capacitor electrode -- shown in the aspect of the invention of Fig. 1.

The remaining claims 64-84 are supported by, for example, originally-filed claims 20-40.

The previous claims of the application were rejected over Raaijamakers, Kim and Lee. The new claims presented herein have limitations not disclosed or suggested by any combination of the cited references, and thus are believed to be allowable.

Respectfully submitted,

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